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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/022,794	12/20/2001	Yoichi Fujita	01-242	3769

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EXAMINER	
SURYAWANSHI, SURESH	
ART UNIT	**PAPER NUMBER**
2115	

DATE MAILED: 12/28/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)
	10/022,794	FUJITA ET AL.
	Examiner	Art Unit
	Suresh K Suryawanshi	2115

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *20 December 2001*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-19* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-19* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *11 March 2002* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *12/20/01*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-19 are presented for examination.

Specification

2. The disclosure is objected to because of the following informalities: symbol "7" should be "6" at page 7, line 18.

Appropriate correction is required.

3. The disclosure is objected to because of the following informalities: symbol "15" should be "150" at page 18, line 7 and line 17.

Appropriate correction is required.

Claim Rejections - 35 USC § 112

4. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

5. Claim 3 recites the limitation "the monitor" in line 11. There is insufficient antecedent basis for this limitation in the claim.

6. Claim 3 recites the limitation "the predetermined input terminal" in line 11 through 12. There is insufficient antecedent basis for this limitation in the claim.

Claim Rejections - 35 USC § 102

7. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

8. Claims 1-19 are rejected under 35 U.S.C. 102(e) as being anticipated by Tetsushi (US Patent no 6,198,820 B1[1]).

9. As per claim 1, Tetsushi teaches

a central processing unit (CPU) [Fig. 7; col. 8, lines 55-56; col. 9, line 1; col. 12, line 19];

a main-clock generating means for generating a main-clock [Fig. 7; col. 8, lines 58-62; a clock of 42 KHz; col. 9, lines 1-14; clock management section; col. 12, lines 28-31; a high-frequency clock oscillator];

a sub-clock generating means for generating a sub-clock of the frequency which is lower than the main-clock [Fig. 7; col. 8, lines 58-62; a clock 32.768 KHz; col. 9, lines 10-14; col. 12, lines 21-22; a low-frequency clock oscillator];

an intermittent operation control means which operates by receiving the sub-clock to control the intermittent operation of the CPU and moreover stops, upon reception of the stop command, operation of the main-clock generating means and starts measurement of the predetermined setting time and moreover starts again, after the setting time has passed, operation of the main-clock generating means to raise the CPU to the operating condition from the stop condition in view of realizing the intermittent operation of the CPU [Fig. 7; col. 9, lines 1-29, 39-44; col. 9, line 66 -- col. 10, line 21; col. 12, lines 35-48]; and

an intermittent time measuring means which operates by receiving the sub-clock to measure the period in which the CPU is in the stop condition by reading such measured value [Fig. 7; col. 9, lines 1-29, 39-44; col. 9, line 66 -- col. 10, line 21; col. 12, lines 35-48].

10. As per claim 2, Tetsushi teaches that the intermittent time measuring means is structured to be set, with an operation mode switching command from the CPU, to any operation mode of a first mode to measure a period in which the CPU is in the stop condition and a second mode to continuously measure the time and to clear the measured value with a clear command from the CPU when at least the operation mode is set to the second mode [col. 9, lines 1-29].

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[1] Tetsushi is a prior art cited by applicants in information disclosure statement (12/20/01).

11. As per claim 3, Tetsushi teaches

a CPU which can operate depending on programs and can stop the operation thereof with execution of the predetermined instruction [Fig. 7; col. 9, lines 1-10], and further comprising:

an automatic signal reading means for reading and determining, when the CPU is in the stop condition, a level of the monitor object signal supplied to the predetermined input terminal of the microcomputer in every constant period and then raising the CPU to the operating condition from the stop condition when the determined level reaches the particular level [Fig. 7; col. 9, lines 1-29, 39-44; col. 9, line 66 -- col. 10, line 21; return position control section works as an automatic signal reading means and determines when to start the high-frequency clock oscillator and the CPU from the stop condition when the determined count level of the 32 K slot counter equals to the slot return position set by the CPU].

12. As per claim 4, Tetsushi teaches that the automatic signal reading means updates the determined level of the monitor object signal to the level read this time only when the level read from the input terminal becomes identical continuously for a plurality of predetermined times [Fig. 7; col. 9, lines 1-29, 39-44; col. 9, line 66 -- col. 10, line 21].

13. As per claim 5, Tetsushi teaches that the automatic signal reading means can be switched to an operation mode for executing a filter process depending on a command from the CPU and an operation mode for setting the level read from the input terminal as the determined level of the monitor object signal without execution of the filter process [Fig. 7; col. 9, lines 1-29, 39-44; col. 9, line 66 -- col. 10, line 21].

14. As per claim 6, Tetsushi teaches that the particular level is set by the CPU in the automatic signal reading means [Fig. 7; col. 9, lines 1-29, 39-44; col. 9, line 66 -- col. 10, line 21].

15. As per claim 7, Tetsushi teaches that the constant time is set by the CPU in the automatic signal reading means [Fig. 7; col. 9, lines 1-29, 39-44; col. 9, line 66 -- col. 10, line 21].

16. As per claim 8, Tetsushi teaches that the automatic signal reading means outputs from the predetermined output terminal of the microcomputer, before reading a level of the monitor object signal from the input terminal, a power feeding signal to supply a voltage to a pull-up resistor for pulling up a signal line for supplying the monitor object signal to the input terminal and stops output of the power feeding signal when the level of the monitor object signal is read from the input terminal [col. 10, lines 22-53].

17. As per claim 9, Tetsushi teaches that a waiting time until level reading of the monitor object signal from output of the power feeding signal is set by the CPU in the automatic signal reading means [inherent to the system as the CPU sets an intermittent receiving control or the slot return position and etc.; col. 9, lines 1-29, 39-44; col. 9, line 66 -- col. 10, line 21; col. 10, lines 35-53].

18. As per claim 10, Tetsushi teaches that the automatic signal reading means can be set, depending on a command from the CPU, to an operation mode in which the power feeding signal output control is not executed [inherent to the system as the CPU sets an intermittent receiving control or the slot return position and etc.; col. 9, lines 1-29, 39-44; col. 9, line 66 -- col. 10, line 21; col. 10, lines 35-53].

19. As per claim 11, Tetsushi teaches that an input terminal with which the automatic signal reading means reads a signal level is set by the CPU to any one of a plurality of terminals of the microcomputer [inherent to the system as the CPU sets an intermittent receiving control or the slot return position and etc.; col. 9, lines 1-29, 39-44; col. 9, line 66 -- col. 10, line 21].

20. As per claim 12, Tetsushi teaches that a timer rise control means for starting, upon reception of an operation request from the CPU, measurement of time which is previously set by the CPU and then raising the CPU, when such preset time has passed, to the operating condition from the stop condition [col. 9, lines 1-29, 39-44; col. 9, line 66 -- col. 10, line 21].

21. As per claim 13, Tetsushi teaches that the automatic signal reading means comprises a read result storage section which stores the level of the monitor object signal determined therewith and allows the CPU to read the stored content [Fig. 7; receiving section].

22. As per claim 14, Tetsushi teaches that the automatic signal reading means can operate with a command from the CPU while the CPU is in the operating condition [inherent to the system].

23. As per claim 15, Tetsushi teaches

a CPU to execute the process in relation to the external apparatus [Fig. 7; col. 8, lines 55-56; col. 9, line 1; col. 12, line 19; the portable remote terminal apparatus turns into the intermittent receiving mode];

an intermittent operation control means for controlling intermittent operation of the CPU [Fig. 7; col. 8, lines 55-56; col. 9, line 1; col. 12, line 19; intermittent receiving control]; and

a timer interlocking control means for outputting the drive signal to the external apparatus depending on the preset time [Fig. 7; col. 8, lines 55-56; col. 9, line 1; col. 12, line 19; the return position control section resets the intermittent enable bit and starts the CPU from the sleep mode to normal mode based on the return timing set by the CPU or in response to the return trigger TR, the portable remote terminal apparatus is switched over to the receiving state].

24. As per claim 16, Tetsushi teaches that the intermittent operation control means operates by receiving a sub-clock in the frequency lower than that of a main-clock for operating the CPU [Fig. 7; col. 8, lines 58-62; a clock 32.768 KHz; col. 9, lines 10-14; col. 12, lines 21-22; a low-frequency clock oscillator].

25. As per claim 17, Tetsushi teaches that the timer interlocking control means operates by receiving the sub-clock in the frequency lower than that of the main-clock for operating the CPU [Fig. 7; col. 8, lines 58-62; a clock 32.768 KHz; col. 9, lines 10-14; col. 12, lines 21-22; a low-frequency clock oscillator].

26. As per claim 18, Tetsushi teaches that the setting time is set for the timer interlocking control means while the CPU is in the operating condition [col. 9, lines 1-29, 39-44; col. 9, line 66 -- col. 10, line 21].

27. As per claim 19, Tetsushi teaches that the setting time is set enough for the external apparatus to complete preparation for process when the CPU rises to the operating condition from the stop condition [inherent to the system to do so and thus not to waste power unnecessarily].

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Suresh K Suryawanshi whose telephone number is 571-272-3668. The examiner can normally be reached on 9:00am - 5:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Thomas C. Lee can be reached on 571-272-3667. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

sks
December 8, 2004

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